

# Synthesis Based Design Techniques for Ultra Low Voltage Energy Efficient SoCs

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## Abstract

Energy efficiency is increasingly becoming the main concern for many emerging system-on-chip (SoC) applications such as those for wireless sensor networks (WSNs) or portable electronics, which require ultra low power and high energy efficiency. Though voltage scaling down to near-(NVt) and sub-threshold(sub-Vt) supply voltages has provided drastic quadratic savings in dynamic energy, design of circuits at ultra low voltages (ULVs) still poses important challenges, and methodologies in their current state still leave much space for optimization.

For the circuits involved in SoCs, exponentially slower speeds in the ULV regime not only mean a limit on the throughput available, but also an increase in the significance of leakage current, which may undermine our purpose of energy efficiency. Increased sensitivity to process variation makes robust timing closure a key challenge at ULVs, which makes it exceptionally hard for industry to accept ULV designs as future solutions because of the low chip yield this entails. As to the SoC architecture, judicious considerations as to the size, amount, type, and communication of modules with respect to energy efficiency must be studied to ensure a deployable design.

In this work, we first investigate the energy efficiency vs. module platform flexibility design space to answer the question how much energy efficiency is available in each type platform (general purpose processor, FPGA, or ASIC) in being the main driving force behind digital processing. Next, we explore if a body area sensor node SoC that uses several circuit and architectural methods and is capable of flexible bio-signal sampling and processing presses the point of minimal energy enough for battery-less operation. We delve into circuit design for ultra low power SoCs, and question the need for a new robust circuit topology to design standard cells for ULV, as well as questioning the need for a standard cell library characterization method that ensures robust operating logic cells. We ponder at whether a method for energy efficient and variation tolerant clock tree design for hold timing closure is needed, and if so what method we should use. And finally, we research to see if using latches in place of registers for both speed and energy optimization can lower the minimal energy point, change the analysis of optimal pipelining, and give light to an alternative approach to dynamic voltage and frequency scaling (DVFS). Our overall hypothesis is that the success of these projects will enable robust, energy efficient designs in the ULV region, and increase the recognition of ULV designs as viable solutions to industry related problems.

# 1 Introduction

## 1.1 Motivation for Ultra Low Voltage Design

A wide variety of emerging applications will require much lower power levels for operation. These applications may range from the ultra low power, low performance area of wireless sensor networks (WSNs)[1][2][3] to energy efficiency constrained, medium performance area of low power microprocessors and SoCs used in smartphones, tablets, PDAs, and other mobile electronics such as [4][5]. Finally, though the ITRS roadmap [6] has pressed the semiconductor industry to continue to design circuits with greater processing FLOPS (floating point operations) at higher speeds with smaller transistors (and thus smaller area), the power wall issue associated with maintaining such scaling is giving ever more increasing concern to its fluent continuation. In fact, recently there has arisen the notion of ‘dark silicon’ [7], where simply put, only a portion of the transistors manufactured onto a chip will be turned on at any moment so as not to surpass the chip’s thermal power budget. Clearly, power and energy efficiency is increasingly a major issue to current and future IC designs.

Supply voltage scaling is a main method designers are using to lower power[8], and increasing is the trend to lower the supply voltage to the regime of near-(NVt) to sub-threshold(sub-Vt). However, transistor characteristics change drastically at these voltages, creating problems for conventional design methods that don’t or can’t take these changes into account. Exponentially slower speeds and reduced drive strengths limit throughput and fanout, which are restrictions standard EDA synthesis tools do not consider. Leakage current is also greatly increased, which is a factor conventional design flows may not consider for performing power/energy aware designs. Increased sensitivity to process variations makes it difficult for circuits to achieve robust timing closure and leaves standard cells prone to static noise margin (SNM) failure. Conventional architectural decisions largely consider energy as a secondary metric of optimization behind speed, so different methods for energy optimization on the architecture level need to be emphasized as well.

Especially concerning is the issue of robustness to variation in ULV regions, which perhaps is the main bottleneck impeding the growth for ULV designs as viable solutions to industry and other real world problems and applications. Therefore, our top level hypothesis is that we may prove the viability of ULV design through design techniques focusing on robustness and energy efficiency that move the design space close to actual real-world deployment.

## 1.2 Key Challenges for Ultra Low Voltage Design

### 1.2.1 Weaker and Unbalanced Drive Strength of Transistors

Transistors operating in sub-Vt follow the drain current equation (1), where  $I_o$  is a constant,  $\eta$  is the DIBL coefficient,  $n$  is a non-ideality factor ( $n = 1 + C_D/C_{ox}$ ), and  $V_T$  is the thermal voltage. Compared to

$$I_d = I_o \frac{W}{L} \exp\left(\frac{V_{gs} - V_{th} - \eta V_{ds}}{nV_T}\right) \left(1 - \exp\left(-\frac{V_{ds}}{V_T}\right)\right) \quad (1)$$

the super-threshold equation where drain current is quadratic to the  $V_{gs}$  term, equation (1) shows the exponential relationship of  $V_{gs}$  to current in sub-Vt. This means that current, of transistors decreases dramatically when in sub-Vt, which in turn means much slower speeds of circuits in sub-Vt. Other than limiting the throughput available in sub-Vt (Fig. 1), the much lower drive strength also poses new challenges of limited fanout and increased leakage in digital circuits. A limited fanout means each logic cell has less capability to span out and drive several logic paths, leading to duplicate logic paths, minimum sized loads, and more complex timing issues, all of which lead to less robust designs and higher energy. To illustrate the difference of drive strength capabilities between super- and sub-threshold, Fig. 2 shows the amount of capacitance an inverter can drive to maintain its FO4 delay across a swept  $V_{DD}$ .  $C_{in}$  was measured using a constant current source to slowly charge the input gate-capacitance of an inverter over a period of time and using  $CV=It$  equation.  $C_{out}$  was measured by calculating the FO4 delay with an inverter driving four replicas of itself, then replacing the four replicas with an ideal capacitance and measuring its value when the driving gate achieved the same propagation delay.

The slower speeds also drastically increase the significance of leakage energy in a circuit (Fig. 3). The reason for this increase is at slower speeds, for each logic cell in a pipeline, once it is finished performing its logic operation, it waits idling until the next clock period where it performs the next logic function. The cell leaks for the entire period while only drawing active current for a small portion of the period. Thus, the penalty of leakage energy is much increased.

Furthermore, due to device characteristics, the relative strengths of PMOS vs. NMOS changes from super- to sub-threshold (Fig. 4). This negatively affects timing in terms of both setup and hold time, as either a 0 or 1 will be much more of a limiting factor to these timing metrics as its counterpart. Circuits also pay the penalty of poor slew (10% of  $V_{DD}$  to 90%  $V_{DD}$  transition time) and increased short circuit power to recover from poor slew. In its extremity, several consecutive poor edges caused by imbalanced pullup/pulldown can lead to an undefined logic state in the ensuing logic gate.

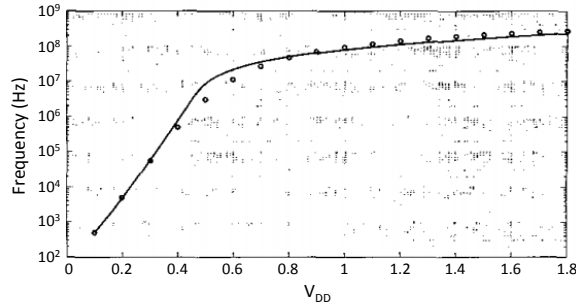


Figure 1. Frequency versus  $V_{DD}$  for FIR filter.  $V_{th}$  is ~450 mV. Taken from [9].

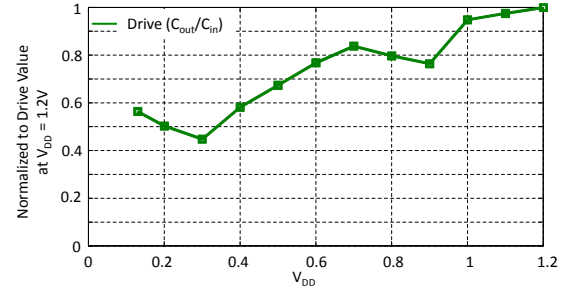


Figure 2. Drive strengths of an inverter over  $V_{DD}$ . Drive is the ratio of  $C_{out}/C_{in}$  at FO4 delay. Non-monotonic trend is due to changing  $C_{gate}$  properties during a transition.

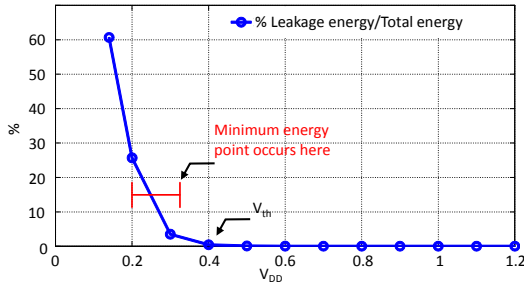


Figure 3. Proportion of leakage energy out of total energy for 16-stage ring oscillator. Simulation results show leakage energy become significant around minimum energy point.

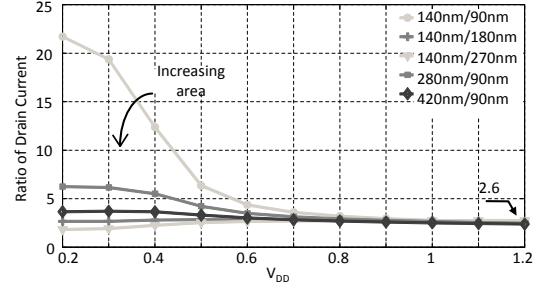


Figure 4. Relative strengths of NMOS vs. PMOS across  $V_{DD}$ . Simulation results from a commercial 90nm technology.

## 1.2.2 Variability

Variation has continued to become a huge challenge with technology scaling. Generally, variation has three main sources from process variation, voltage supply fluctuation, and temperature change (PVT variations). What's more, the impact of PVT variations is exaggerated at ULVs. Random dopant fluctuation's (RDF) effect on  $V_{th}$  (threshold voltage) can be modeled as a normal distribution with the standard deviation inversely proportional to transistor channel area. From equation (1) we can see this means  $I_d$  has a log-linear distribution, leading to much more spread out distribution tails for various important metrics (Fig. 5). What's more, to control RDF we must upsize the gate, meaning increased energy and a penalty to our purpose of energy efficiency. Since the  $V_{gs}$  term in equation (1) also resides in the exponential, supply variation too has a drastic effect on the amount of current and delay through gates. Finally, since both  $V_T$  (thermal voltage) and  $V_{th}$  vary with temperature, delay distributions have strikingly different attributes based on temperature, as shown in Fig. 6.

## 1.2.3 Energy Efficient Hardware Selection

Though SoCs have long existed for their advantages in high-integration, low module to module communication cost, and smaller size[10], their optimization has largely centered around the topics of speed and communication/memory bandwidth. However, applications that require prolonged battery lifetime like wireless sensor networks for health monitoring and actuation[1] or mobile electronics like cell phones and tablets[11] place great emphasis on optimized energy consumption to meet application characteristics. With so many modules on chip, the communication cost can be extremely high if a correct bus protocol is not designed. Depending on application characteristics, either a flexible microcontroller (MCU) that consumes more energy or a highly energy efficient but application constrained ASIC may be the optimal choice to carry the signal processing load of the SoC. Therefore, for the emerging area of energy efficient applications, the challenge of designing energy efficient architectures and choosing energy efficient modules remains a space to be explored.

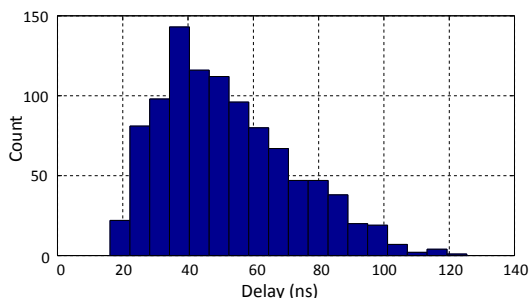


Figure 5. 1000 point Monte Carlo simulation results for delay of a string of 4 inverters where  $V_{DD}=0.3V$ . Probability distribution displays log-linear characteristics.

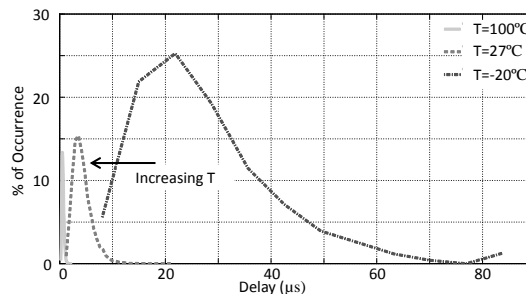


Figure 6. 10,000 point Monte Carlo simulation results for delay of 10 inverters where  $V_{DD}=0.3V$  at 3 temperatures (T). Distribution drastically changes across different T.

### 1.3 Goals

Our work will address some major difficulties of ultra low voltage energy efficient SoCs. We will focus on the integration of methodologies to choose and design an energy optimal SoC architecture and the modules that comprise it. We will also focus on circuit techniques that cater to the relatively new ULV design regime, especially focusing on our high level goal of robustness and high energy efficiency. Though we understand that a thorough treatment of viability for ULV design deployment would entail research into a broader range of topics such as memories, power delivery, interconnect effects, etc., we have chosen our subset of topics (standard cell library robustness, leakage optimization, timing closure, and timing schemes) because they deal with core aspects of making large scale digital integration possible. The major goals of our work are:

- Investigate how to build an ultra low power, energy efficient SoC. Propose a design architecture that stresses minimum energy and evaluate it by determining if such a design is low power and low energy enough to run without a battery (run off of harvested ambient energy).
- Propose standard cell designs that fit needs at ULVs which withstand PVT variations and minimize total energy. Evaluate the new cells against conventional static CMOS with respect to delay, leakage energy, and total energy for a given yield constraint. Does the new method consume less total energy for a given yield aim?
- Investigate a methodology that captures reliable timing information during cell library characterization for synthesis. Evaluate the method against conventional EDA tool supplied method in terms of yield of circuit achieved and time to characterize/design. Does the methodology give reliable timing information that increases the circuit yield compared to without the method?
- Propose a methodology for robust hold-time timing closure in sub- $V_t$  that determines the clock tree design, register design, and amount of hold buffering needed with respect to meeting a yield constraint using the lowest energy possible. Compare the method with conventional EDA supplied methods with respect to yield and total energy of circuit.

- Investigate a novel solution to hold-time PVT variation robustness. Evaluate the solution by comparing to other state-of-the-art solutions in terms of circuit yield and total energy.
- Analyze the optimal level of pipelining in terms of minimum energy achievable given a throughput constraint for a circuit when using latches in place of registers. Evaluate this design scheme by comparing against conventional register based designs with respect to energy, delay, and complexity of timing closure.
- Investigate a novel alternative to DVFS (dynamic voltage and frequency scaling) using a dynamically switched level of pipelining in a circuit. Evaluate the novel approach against state-of-the-art DVFS approach(es) in terms of total energy consumed through the DC-DC converter(s), total system complexity, and ease of dithering.

**Problem statement:**  $V_{DD}$  scaling down to near- and sub-threshold region is desired for ultra low power SoCs, but such circuits are limited because of longer delays, increased leakage current and increased sensitivity to PVT variations. New techniques must be provided to deploy energy efficient and more robust designs that trend toward commercial deployment and widespread adoption.

## 2 Hardware Selection for Energy Efficient SoC

### 2.1 Motivation

Many emerging embedded application have stringent power and energy requirements to meet battery life and size constraints. An example application that takes these constraints to the extremity is long-term medical devices and wearable devices. Therefore, it is imperative, when thinking about the architecture of a SoC and the variety of components on it, to make judicial decisions to which components to include so that their energy efficiency is optimized while still meeting the throughput and processing capability requirements of the application. Where in economics we want to ‘make every dollar count’, for a SoC we wish to ‘make every pJ count’.

Recent advances in ultra-low power chip design techniques have potential to realize a new generation of superior energy efficient SoCs. However, there remains the difficulty of determining what combination of hardware modules maximize energy efficiency given a variety of application based processing capabilities, which is the main issue we deal with in this Chapter. This is especially true for the digital components on a SoC, as their selection spreads from the highly flexible but inefficient general purpose processors (GPPs) to the highly efficient but non-flexible ASIC accelerator modules.

### 2.2 Related Work

The tradeoff between flexibility and efficiency in hardware is well known and very prominent in a comparison of conventional hardware paradigms[12][13]. The most flexible category of hardware is general purpose processors (GPPs). GPPs exhibit poor energy efficiency due to the overhead of fetching and decoding the instructions that are required to perform a given operation in the datapath[14]. Sophisticated operations like a fast Fourier transform (FFT) or data processing algorithm will thus require numerous instructions in a simple core. For example, several sub-threshold processors provide energy per instruction nearing 1 pJ per operation, but they also tend to use small instruction sets and thus result in more instructions to run an operation.

The most efficient hardware is hardwired to do its specific task or tasks (e.g. ASIC). ASICs achieve very efficient operation, but they can only perform the function for which they were originally defined. Examples of hardwired implementations in sub-threshold circuits include [15][16]. Different types of hardware in sub-threshold systems reveal a similar trend as their above-threshold counterparts. Some chips may be implemented as complete ASICs like JPEG or FFT processors, but more commonly the case for SoCs, ASICs may appear as auxiliary hardware accelerator modules, performing commonly occurring

functions in the context of the larger system. Good examples of hardware acceleration are multipliers, floating point units, or FIR filters. These operations can take several instructions over many clock cycles to complete using a GPP, consuming a large amount of energy and time. A hardware accelerator can process data quickly and efficiently.

## 2.3 Hypothesis

We hypothesize that by building a body area sensor node (BASN) SoC chip that uses conclusions from a hardware platform comparison study and whose architecture takes into account both flexibility and energy efficiency in data processing, we can achieve a design geared for a variety of ultra low power medical applications that consumes minimal energy that it can operate without a battery, and solely from an energy harvesting source.

## 2.3 Approach

### 2.3.1 A Hardware Platform Comparison

To better understand the energy vs. flexibility tradeoff, we propose a study of three platforms: GPP, FPGA, and ASIC accelerator. To put this comparison in fair context with ultra low power SoCs (perhaps for biomedical purposes), we implemented the same heart rate extraction algorithm (RR extraction) on all three. We also manually implemented all three platforms in the same technology and used the circuit optimization techniques available to us for a custom energy efficiency implementation. Specifically, we used a synthesis flow where cells were characterized at the ULV voltage, manually instructed the RTL translator to use the smallest cells to reduce leakage, and used extensive guardbanding in timing closure for the ASIC and GPP designs. We used a state-of-the-art ULV design for the FPGA [17]. We hand optimized the assembly code for the GPP, and hand optimized the verilog circuit model to ensure we had accomplished the most energy efficient implementation for each platform. We then performed Spice simulation of our circuits and verified correct functionality of execution of our RR algorithm, and extracted our key metrics of energy/op, delay, and # of instructions per processed sample.

### 2.3.2 Platform Evaluation

The results of our experiment are presented in Table 1. The key observation is that there is a drastic improvement in efficiency (>100x) between GPPs and FPGA/ASICs. Therefore, it makes sense to assign the bulk of processing duties to FPGA and ASIC platforms, while using GPPs strictly for control or rarely occurring subroutine operations. This is the key conclusion that our BASN chip will utilize.

**Table 1.** Comparison of different hardware platforms

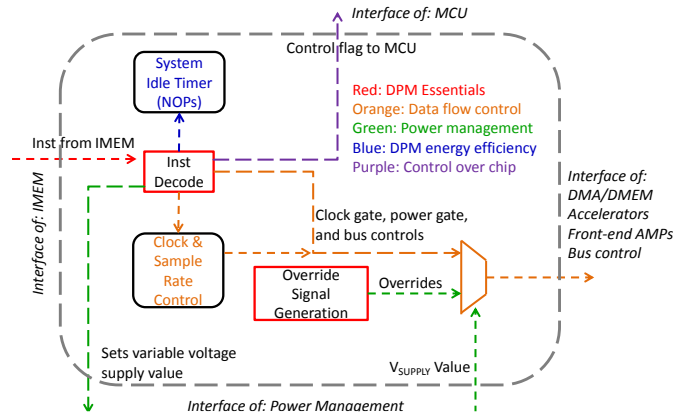
	Energy per Instruction	Energy per Sample	Delay per Sample	Max achievable data rate	GOPS / W
GPP (from[ref])	2.62 pJ	210 pJ	8 us (80 cycles)	125 kHz	4.76
FPGA(from[ref])	N/A	2.22 pJ	94.5 ns (1 cycle)	10 MHz	450
ASIC	N/A	0.23pJ	6.18 ns (1 cycle)	150 MHz	4348

### 2.3.3 An Ultra Low Power Body Area Sensor Node

Recent advances in ultra-low power chip design techniques, many originally targeting wireless sensor networks(WSNs), will enable a new generation of body-worn devices for health monitoring. We recognize this as an opportunity to explore the design space where energy efficiency is pressed to the extreme. With state-of-the-art in low power RF transmitters, low voltage boost circuits, subthreshold processing, biosignal front-ends, dynamic power management, and energy harvesting, we propose to realize an integrated reconfigurable wireless body-area-sensor node (BASN) SoC capable of autonomous power management for *battery-free* operation. This will require careful scrutiny over how power is

managed, which modules/platforms should go on-chip for most efficiency, and how numerous blocks interact and communicate with each other.

Our targeted application requires implementation of specific algorithms for atrial fibrillation (AFib) and muscle movement, or electromyography (EMG) band energy detection. Once the algorithm is determined for these, an ASIC implementation can proceed. Yet, the need for broader capabilities of the SoC to justify causes such as commercialization or flexibility poses the challenge for putting generic processing modules on chip as well. Therefore, GPPs are needed. We propose an architectural decision to solve this problem like one shown in Fig. 8. Both accelerators and a GPP are implemented, but depending on the desired algorithm, a module called the digital power manager (DPM, Fig. 7) can be programmed to control the data flow on-chip and judiciously choose which modules to perform the processing task, according to the conclusion of Section 2.3.2.



**Figure 7. Block diagram of DPM in [1].** The DPM acts like a GPP and controls data flow, power- and clock-gating, and sample rate on the chip (red & orange). Therefore, energy efficiency is achieved by allowing accelerators to perform processing. The DPM also implements a closed-loop power management scheme and controls voltage regulation (green). It also sports a low power idle mode (blue). If extra flexibility is desired, it may hand control over the chip to the MCU (purple).

Another design challenge needing to be addressed is that of power management. Since the SoC is battery-less and running off of harvested energy, we propose that the DPM also overrides the clock and power gating from the program so that the chip does not consume too much energy than stored from harvesting and ‘die’. The sizes of the instruction memory (IMEM) and data memory (DMEM) were carefully chosen to incorporate a large range of memory needs but not more so to keep memory leakage at a minimum. Since data memory access latencies can be long and the timing confusing to the DPM, who already must keep track of numerous items, all DMEM accesses are done through a DMA accelerator. To provide flexibility in sampling rate, the clock periods of all accelerators are programmable through a clock arbiter accelerator. It is known that bus communication, especially those done through handshaking are energy hungry, so to alleviate this problem, the bus for the SoC is implemented as a simple direct-addressed tri-gate ‘switch-box’ controlled by the DPM. In the end, the DPM becomes a custom ISA always-on ‘brain’ for the SoC. The resulting whole chip architecture with analog portions we propose is also shown in Fig. 8.

## 2.4 Goals and Contributions

### 2.4.1 Current Results

The proposed chip was fabricated in a commercial 130nm process. Digital portions were synthesized using the same optimized sub-Vt synthesis flow as described in Section 2.3.1. All 10 test chips returned were verified for functionality and all passed[1]. An ECG experiment was performed on a healthy human subject. First, the chip was set to ECG raw data mode (consuming 397 $\mu$ W from the 1.35V  $V_{BOOST}$  node). Data was transmitted to a TI CC1101 receiver, and the reconstructed ECG was found to closely match the actual ECG. Next, the chip used the on-chip R-R interval extractor to transmit measured heartrate every (650 $\mu$ s including turn-on time and transmitting 24b).



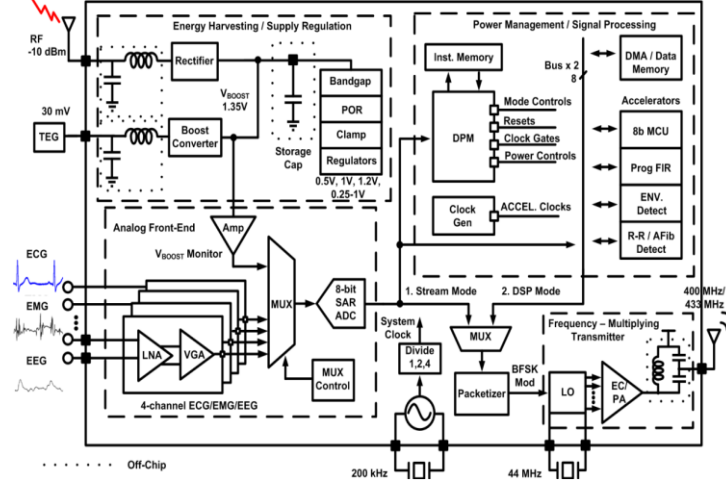


Figure 8. SoC architecture of [1]. Chip integrates energy harvesting, power management, low power data acquisition, flexible DSP, and selective transmission for a battery-less solution for various medical applications.

The heart rate extractor algorithm measures the R-R interval with a time resolution of  $(1/128)s$ . In AFib detection mode, the R-R and AFib accelerators enable the TX and transmit the last 8 beats of raw ECG (buffered in the data memory) only when a rare AFib event occurs (Fig. 10). The total chip power in both the R-R and AFib modes is  $19\mu W$ , sufficiently low enough power to be supplied from the energy harvesting thermo-electric generator (TEG).

A performance comparison table is presented in Fig. 11, highlighting the contributions of this chip. To the best of the authors' knowledge, this system has lower power, lower minimum input supply voltage, and more complete system integration than all other reported wireless BASN SoCs. Fig. 12 shows the micrograph of the  $2.5mm \times 3.3mm$  chip (130nm CMOS). This work presents the first wireless biosignal acquisition chip powered solely from thermoelectric harvested power and/or RF power with integrated supply regulation, AFE, power management, DSP, and TX.

#### 2.4.2 Anticipated Contributions

Since the whole chip is powered from a TEG, the chip is in danger of losing enough power to sustain itself. In this case the program in the IMEM and any processed data in the DMEM will be lost. We propose another BASN SoC with a custom ultra low voltage programmable non-volatile memory (NVM) (industry supplied) to solve the problem of the node 'dying' and being able to 'resurrect' itself. Currently this chip has been taped out and the chips are under test.

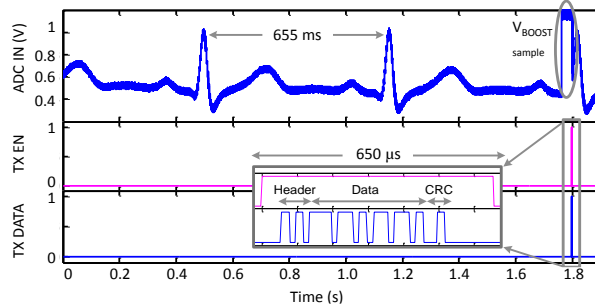


Figure 9. Chip demo where R-R interval is calculated using the MCU and transmitted every 5s. DPM checks  $V_{BOOST}$  every time before transmission.

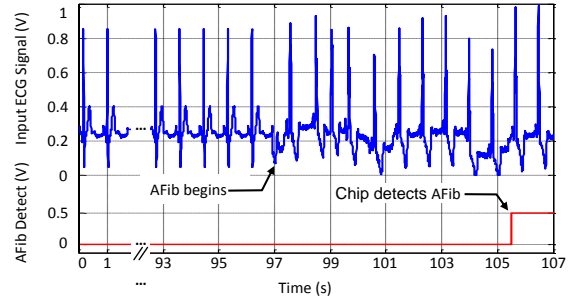
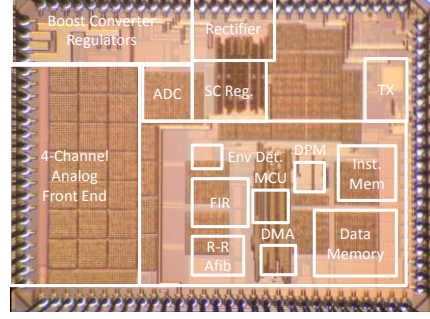


Figure 10. Chip demo where 8 heart beats are buffered in DMEM, and only transmitted when a rare AFib event occurs.



	This Work	[18]	[19]	[20]	[21]	[22]
Sensors	ECG, EMG, EEG	ECG	Neural, ECG, EMG, EEG	EEG	ECG, TIV	Temp, Pressure
Supply	30mV, -10dBm	1.2V	1V	1V	1.2V	0.4V/0.5V
E Harvesting	Thermal, RF	X	X	X	X	Solar
Power Mgmt.	DPM, Clock/Power gate	Clock gate	X	X	X	Power gate
Gen. Purp. MCU	1.5 pJ/Instr @ 200kHz	X	X	X	X	28.9pJ/Instr @ 73kHz
Accelerators	Many	ASIC	X	ASIC	Few	X
Memory	5.5kB (0.3V-0.7V)	42kB (1.2V)	X	x	20kB (1.2V)	5kB (0.4V)
Digital Power	2.1μW	~12μW	N/A	2.1μW	500μW	2.1μW
Total Power	19μW	31.1μW	500μW	77.1μW	2.4mW	7.7μW

**Figure 11. Performance comparison between [1] and recently published BASNs.**



**Figure 12. Annotated die photo of BASN chip[1].**

## 3 Library Design and Characterization at ULVs for Robust Timing Closure

### 3.1 Motivation

Standard cells are the building blocks of large integrated digital circuits. Components and whole SoCs are realized through a design flow process called synthesis where tools will ‘automatically’ build circuits using standard cells based on the description of their logic (written in verilog or VHDL). It can be said that standard cells are key components to the design process, functioning as the Lego blocks of the VLSI world.

While the design process of standard cells, whether they be basic logic gates (NAND, NOR, INV, etc.) or state saving components (LATCH, REG, etc.) or other ‘gadget’ type components (TRI-GATE, CLOCK-GATE, etc.) is well established for super-threshold, it is largely not optimized for ULV regimes.

Simply using industry established standard cell libraries scaled to ULVs will result in imbalanced cell delay metrics for 1’s and 0’s because the PMOS vs. NMOS strengths change. Since delays are much longer in sub-Vt, cell leakage becomes a much more important metric. However, this effect is neither captured in the cell characterization step, nor optimized in the cell design itself. PVT variations cause major issues for standard cells. Stacked transistors have a much greater chance of failing SNM, and timing characterization can become unreliable due to PVT variations. Thus, it is imperative that standard cell libraries are relooked for balance, optimized leakage, and robustness to PVT variations for sub-Vt, which are issues this Chapter deals with by proposing designing with transmission-gate style standard cells for sub-Vt standard cells.

What’s more, though there has been recent research on building the right library for sub-Vt or statistical methods to evaluate yield for timing closure, we are lacking in an integrated approach to timing closure when using these libraries in a full synthesis flow. Thus, we propose a wholly integrated timing closure flow that takes advantage of improved cell design strategy for sub-Vt, is variation aware, and optimizes leakage energy, which is the main contributor to energy in non-critical timing paths.

### 3.2 Hypothesis

We hypothesize that by designing standard cells using a transmission-gate based style geared for sub-Vt, we will have lower energy consumption for a given throughput and yield constraint for sub-threshold circuits when compared to conventional static CMOS counterparts. Or, an analysis of where and how conventional static CMOS gates fail can inform when a change in logic style is needed to ensure robust cells in sub-Vt. By using a cell characterization method that better estimates logic delays in face of PVT variations, we hypothesize to gain an improved timing closure yield compared to the EDA method of characterization. Using a synthesis flow that lowers leakage energy by identifying non-critical paths and sacrificing speed for better leakage on those paths, we can achieve lower total circuit energy when compared to the standard EDA synthesis flow.

### 3.3 Approach

#### 3.3.1 Characterizing the Key Challenges

The balancing of pull-down and pull-up network poses an interesting problem for sub-threshold design. Fig. 13 shows the relative achievable speed of a 16-stage ring oscillator designed through an industry supplied standard cell library and one custom sized for sub-threshold (still static CMOS) at iso-energy/cycle across  $V_{DD}$ s. As can be seen, the different sizing methods fare well only in their respective regions. The sub-threshold sizing of gates slows the circuit  $\sim 20\%$  at nominal  $V_{DD}$ , but speeds the circuit up  $\sim 20\%$  in sub-threshold. Fig. 14 shows the yield of scaled standard cells with respect to SNM. These results are optimistic, since all the gates are unloaded and simulated at TT corner, and thus cause concern since some common cells can't even pass SNM test with favorable conditions. Fig. 14 also shows three main failure mechanisms in sub-threshold: bad feedback and cross-coupled hold logic sizing (DFF), bad multi-stage logical effort sizing (XOR2), and large PMOS/NMOS (in this technology, PMOS are much weaker than NMOS in sub- $V_t$ ) imbalance (NOR2). Fig. 15 shows the effect of channel area on variability. Though greater channel area decreases variability ( $\sigma/\mu=0.24$  for  $L=90\text{nm}$ , and  $\sigma/\mu=0.15$  for  $L>90\text{nm}$ ), this knob is much less effective after a certain area has been reached, and comes with costs such as greater delay and energy, both due to increased capacitance. Fig. 16 displays variability against logic depth, and suggests that variability worsens with deeper logic depth.

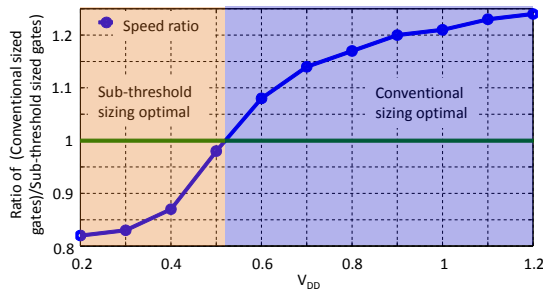


Figure 13. Speed ratio of 16-stage ring oscillator between (Conventional sized gates)/(Sub-threshold sized gates). Both sizing are done at iso-energy/cycle.

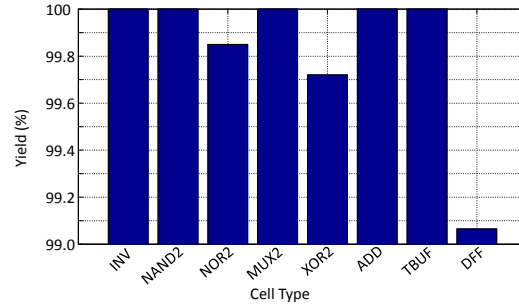


Figure 14. SNM yield of common sub-threshold standard cells simulated with 10,000 point Monte-Carlo where  $V_{DD}=0.25\text{V}$  at TT corner. All gates are unloaded.

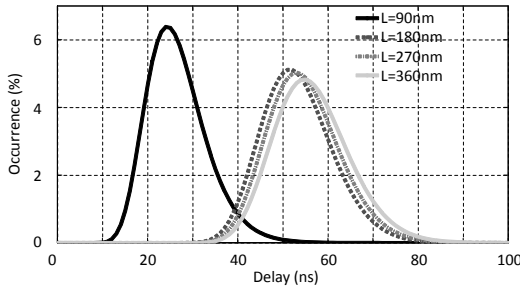


Figure 15. Variability of inverter with different lengths at  $V_{DD}=0.25\text{V}$  and iso-drive current. Greater channel area limits variability, but at a delay penalty.

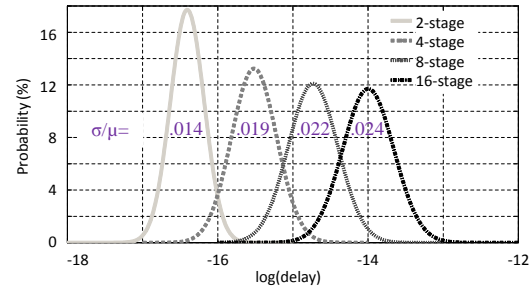


Figure 16. Variability vs. logic depth. Logic paths modeled through inverter chains each driving a FO4 load at  $V_{DD}=0.25$  where input slew and output load are constant.

### 3.3.2 Related Work

[23] presents a sub-threshold cell sizing methodology that has better balance than conventional sizing and takes care of the inverse narrow width effect (INWE). Though they do not discuss robustness in the face of PVT variation, their method should be kept in mind when exploring our topic. [24] also presents insights into sub- $V_t$  standard cell library sizing with regards to variation, and hints that pass-transistor logic fares quite well in sub- $V_t$ . [25-27] discuss systematic, post standard cell design methods to statistically arrive at robust timing closure. [28][29] derive sub-threshold leakage and sizing models for sub-threshold stacked transistors. Lastly, [30-32] talk about low power register design, perhaps one of the most difficult commonly used cells to design because of the multiple stacked transistors and feedback loops in registers.

### 3.3.3 Proposed Research Steps

We propose an integrated timing closure and synthesis flow for sub-Vt that is variation aware through customized closure methods for hold or setup critical paths, and leakage aware through using low-leakage custom cells for paths that are non-critical. Fig. 17 shows a flow diagram summarizing the proposed idea. First, we propose to explore the advantages of designing a transmission-gate based standard cell library for sub-Vt purposes, including a thorough review of transmission-gate (TX-gate) logic, and an analysis of the difference between TX-gate style and static logic. Transmission-gate based logic has the advantage of getting rid of stacks in logic gates, and thus has the potential for higher SNM yield. Second, we will design gates with increased length. Though conventionally this increases delay and active energy, longer lengths drastically decrease leakage current. Thus, non-critical timing paths that use these cells may actually cost *less* energy per cycle depending on the clock frequency. Third, we will design two types of sub-Vt robust registers: one optimized for setup time, and another optimized for hold time. Fourth, we propose the integration of this library in RTL synthesis. We run the ‘normal’ RTL synthesis to create a gate netlist. This netlist is simulated to achieve rough estimates of switching activity (which is an important metric that will effect active energy/leakage energy ratio), and hold and setup critical paths. We then run a designed script to replace all the ‘normal’ gate cells with ones in our custom library that will benefit total energy and yield where appropriate. Fifth, we will ask place and route (P&R) tools to retime our circuit with our custom cells, wire loads, and clock tree. Sixth, a custom script flow will extract the clock network, simulate it, and report its effect on timing closure and suggest changes in the clock network. Seventh, our circuit will be retimed with a custom script taking into account the clock network effects and improved clock network. Eighth, and finally, our complete circuit will be simulated for yield, speed, and power/energy and compared with the ‘normal’ resulting designs of a standard flow.

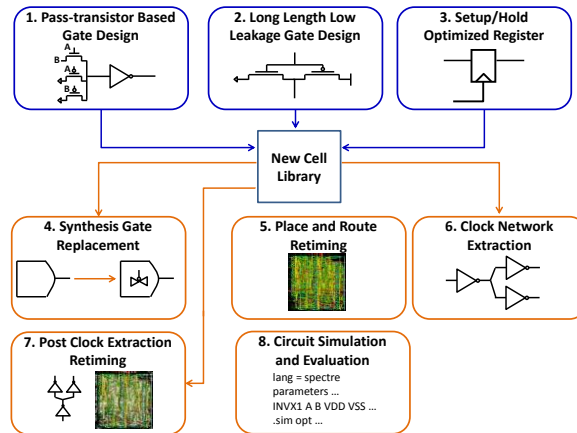


Figure 17. Diagram for proposed library design and characterization flow for sub-Vt synthesizable circuits. Flow starts from re-design of a standard cell library for optimization in variation, balance, and leakage. Then, the resulting designed library becomes part of a custom synthesis flow that utilizes the library at strategic stages for energy/power and variation optimization of the whole circuit.

### 3.4 Goals and Anticipated Contributions

The major goals of this Chapter are to design a transmission-gate based standard cell library, design robust registers for sub-Vt, expand the cell library with greater-length logic gates for leakage optimization, make a cell characterization method that gives better confidence to the statistical nature of gate delays, and design a synthesis flow that identifies non-critical paths and improves the leakage energy for those paths. The results of this project can greatly increase the chip yield for ULV SoCs. For example in the case of the BASN chip, it can be anticipated that mass production of it or similar ultra low power SoC designs would result in much improved yield, as well as drastic decreases in leakage energy.

## 4 Hold Time Analysis and Timing Closure Method for Sub-threshold

## 4.1 Motivation

Since timing closure is imperative for any digital circuit to operate correctly, it is vital that the synthesis flow is re-looked and modified at ULVs to guarantee a robust design. As mentioned commonly in previous chapters, PVT variations are the main culprit to compromised robustness. In our case, they translate to heightened failure rate for hold violations, as contamination delays can be much faster, clock slew much slower, clock skew much higher, and hold robustness of registers much less. Hold time timing closure is an important aspect for various designs, such as re-order buffers or portions of reservation tables and other similar constructs that have shift-register-like functionality. Thus, the aim of this project is to come up with a design methodology that improves robust hold-time closure in spite of these heightened effects of process variation using the least power possible.

## 4.2 Hypothesis

We hypothesize that through analysis of the different metrics involved in hold timing closure (register hold time, clock-q delay, clock skew, clock slew, data slew, and hold buffer insertion) and/or through a novel timing scheme, we can achieve a design methodology that allows a circuit to consume less total energy for a given hold time yield constraint when compared with available EDA tool methods and other state-of-the-art methods.

## 4.3 Approach

### 4.3.1 Key Challenges and the Need for Alternative Hold Time Closure Method

Fig. 18 – Fig. 21 show the main failure mechanisms for hold violations. All circuits simulated were 128-stage shift register blocks using supplied standard cells scaled to sub-Vt. Fig. 18 infers that clock skew is a major issue for hold time. It suggests that the deeper the clock tree, the more skew there is in presence of PVT variations, and thus the lower hold yield. Therefore, the level of clock tree should be kept at a minimum, contrary to clock synthesis methods in super-Vt. Fig. 19 hints at the potential drastic power overhead that hold buffer insertion can impose on a hold critical path. The results are worrisome, since not only do these buffers incur energy overhead, but even when drastic buffer insertion is performed, the timing path yield does not improve to a robust level. In fact, the more heavily we push for higher yield, the overhead increases in a greater than linear pace. Fig. 20 displays how hold violations occur because of poor clock slew. Though the hold time metric for the register doesn't change across slew, the  $t_{c-q}$  time varies greatly with poorer slew, to the extent that contamination delays may be negative (clock-to-q is achieved *before* the clock reaches  $1/2V_{DD}$ ), and the data signal races to the ensuing register causing

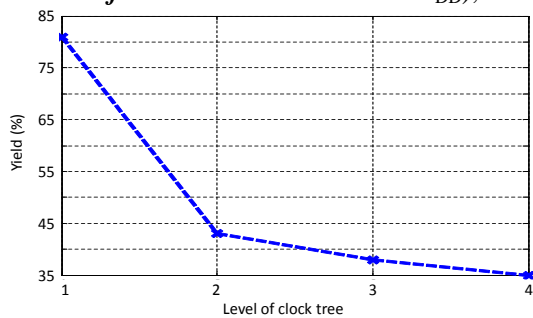


Figure 18. Effect of PVT varying skew on 128 stage shift-register hold time yield. Circuits simulated in 45nm PTM where only the threshold voltage is varied.

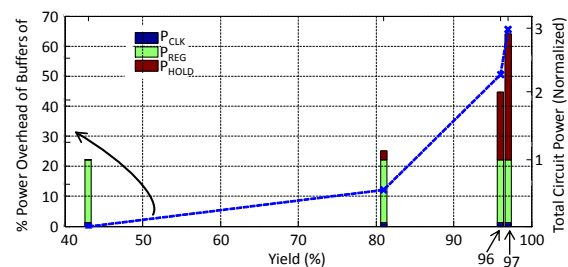
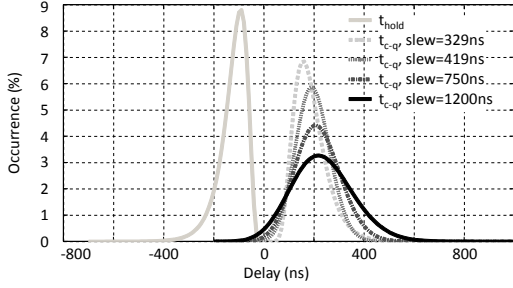
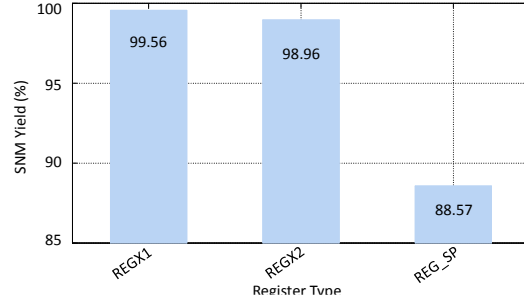


Figure 19. Energy overhead of buffer insertion for hold time fixing. Circuits simulated in 45nm PTM where there are 2 levels of clock tree skew.



**Figure 20.** Distributions of  $t_{\text{hold}}$  and  $t_{c-q}$  with different clock slews at  $V_{DD}=0.25V$ . A cross between a  $t_{\text{hold}}$  and  $t_{c-q}$  curve signifies a definite chance of hold failure.



**Figure 21.** SNM yield rate for commonly used registers. The REG\_SP is a ‘special’ register custom sized for better hold margins and lower power, but has the lowest yield margin.

a hold violation. This phenomenon is worrisome, because clock skew requires us to have less levels of clock tree buffering, while clock slew requires us to have more levels of clock tree buffering to ensure acceptable slew. Therefore, there is a tricky dilemma in the design of the clock tree network, and better clock buffers as well as a judicial topology decision must be made. Lastly, Fig. 21 is telling that the registers themselves must be re-designed as well. In Fig. 21, REGX2 has better nominal hold margin ( $t_{c-q} - t_{\text{hold}}$ ), but fails to provide us with greater hold yield because it has lower SNM yield, most likely caused by imbalanced sizing for sub- $V_t$ . Even more so is the situation for register REG\_SP, which was custom sized for optimal hold margin in sub- $V_t$  at iso-energy/latch when compared to REGX1.

Though it should be noted that the results shown in Fig. 18 and Fig. 19 are pessimistic because they are taken from simulations of circuits designed from the 45nm PTM PDK, which has been found to be overly pessimistic in modeling PVT variations, they still show the potentially drastic negative effects conventional synthesis methods can have in sub- $V_t$ . This observation, along with the difficulty associated with designing better clock buffers and clock topology, motivates us to explore the possibility of a novel hold timing closure mechanism tailored for sub- $V_t$ , which is introduced in Section 4.3.3.

#### 4.3.2 Related Work

Several areas of ground work have been studied as a starting point because of the multi-dimension nature of the problem, and to the author’s best knowledge, neither a comprehensive analysis of the problem of hold time in sub- $V_t$ , nor a dedicated, robust solution has been fully published. [33][34] provide insight into design techniques and points of consideration for lowering variation in sub- $V_t$  designs, while [35][36] gives a thorough analysis as to how common timing paths perform in sub- $V_t$ . [37] gives us a reference point for hold optimal registers, though we must make our own design that is SNM robust as well, and SNM is discussed in [38]. [39] analyzes the effects of increased transistor length, one of the critical methods of increased hold margin which was also used in designing REG\_SP. [40] gives an in-depth treatment of clock tree synthesis for sub- $V_t$ , though they mainly target controlling skew. Finally, [41][42] gives us references for low power all-digital delay-lock loop (DLL) design, which will become an important component within our proposed novel hold timing closure method.

#### 4.3.3 Proposed Research Steps

We propose a comprehensive analysis on the problem of hold time violations in sub- $V_t$  and to derive a strategy that implements low power, high yield hold time timing method with respect to the challenges the variables clock skew, clock slew, data slew, energy overhead of buffer insertion, and register SNM robustness present. We will use the hold time optimized and variation robust register from the results of Chapter 3. First, we propose a thorough analysis of the effects of the variables in question on hold time yield. We then propose to derive a comprehensive design methodology starting with controlling the most sensitive variable (measured as %improved hold yield/energy overhead to control the variable) and moving down the list. The proposed aim is to have this methodology describe a more power and/or energy efficient method to do synthesis using standard EDA tools given a (high) yield constraint. Third, using this methodology as a reference point, we will continue to explore if a novel two-phase clock timing



scheme for hold time fixing may present a better result. Fig. 22 summarizes the broad research ideas of this Chapter, as well as a quick overview of the proposed timing scheme. We hypothesize that the two-phase clock scheme has a high chance of succeeding because with the help of a DLL the pulse-timing

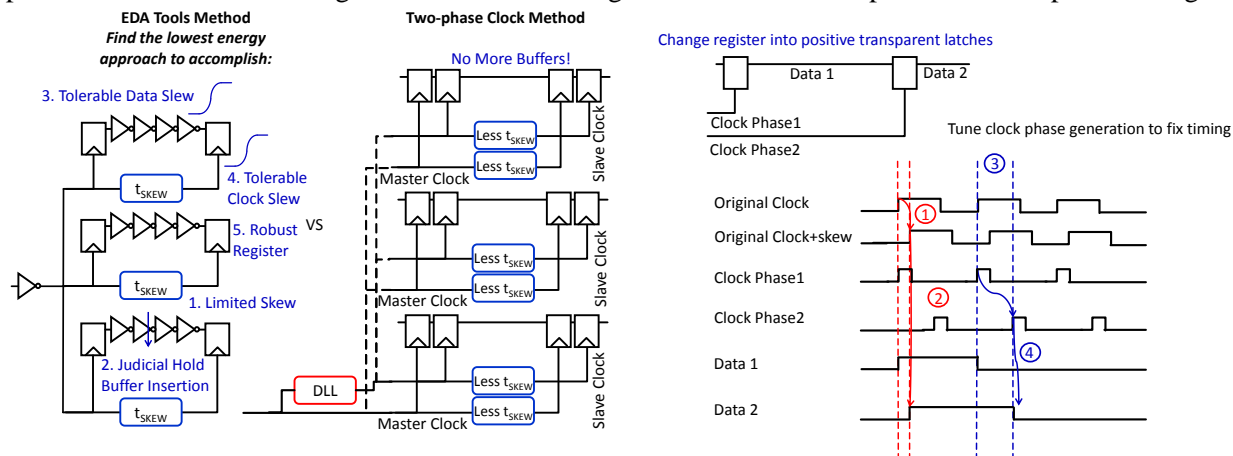


Figure 22. (Left) diagram shows concepts of research proposed this Chapter. We hypothesize that in order of decreasing sensitivity, the important variables are skew, buffer insertion, data slew, clock slew, and register robustness. (Right) shows our proposed two-phase clocking scheme. ① shows an example case where, if we didn't implement our scheme, because of clock skew, Data1 races to Data2 causing a hold fail(②).③ shows an how our scheme would work, and ④ shows the right transition.

involved is much more robust and clearly defined than clock- and hold- buffer delays. Finally, we propose to evaluate the two methods as an integrated system, i.e., clock tree power/energy will be considered for the EDA tool method, and DLL power/energy will be considered for the two-phase clock method.

### 4.3 Goals and Anticipated Contributions

The major goals of this Chapter are to derive a sensitivity list for the variables associated with hold timing failures, come up with a design methodology using EDA tools that improves hold yield by controlling each variable in order of most to least sensitivity, design a novel hold time fixing scheme using two-phase clocking, and evaluate which of the two (EDA tools with sensitivity analysis, or novel two-phase clock scheme) is more energy efficient given a hold time yield constraint. The results of this project are profound, as hold critical, shift-register like constructs appear frequently. For example, in the BASN chip in Chapter 3, components like the DMA, packetizer, and various logic that hold programmable values as in the FIR and envelope detector would benefit greatly from this project, enabling them to deliver functionality with more robustness in an energy efficient manner not requiring guardbanding.

## 5 Latch Based Design for Single- $V_{DD}$ Alternative Approach to DVFS

### 5.1 Motivation

Dynamic Voltage and Frequency Scaling (DVFS) is a concept that has been growing in popularity over recent years. DVS centers on the idea that an abundant amount of applications, especially those designed for mobile platforms and SoCs, have time-varying workload requirements. Take, for example, the processor for a smartphone, which spends a great amount of time idling when the phone is in sleep mode, but runs close to maximum processing ability for the short time one is playing a graphic heavy game. Designing such systems in a static fashion to support the peak performance can lead to substantially increased total system power. DVFS provides the ability to trade-off energy and delay to cater to variable workloads (Fig. 23).

Recent research has demonstrated near ideal energy savings using this concept by using three voltage islands (Fig. 24[44]). However, a potential drawback to such an approach is the consideration of DC-DC converters, which are widely known for having the highest efficiency of voltage regulation. It can be

shown (Fig. 25) that the addition of DC-DC converters may undermine the optimal savings of such schemes. The data points for Fig. 25 were attained by taking the energy points of Fig. 24 and dividing by the highest reported ULV DC-DC converter efficiency report to date[45] where  $\eta=0.7$ . The drop in efficiency is due to the converter not being tuned to the circuit load at a particular  $V_{DD}$  in question, which is inevitable when more than one  $V_{DD}$  is involved. Therefore, if possible it is desirable to achieve a method of ‘DVFS’ that utilizes only one voltage domain where the converter can be fine-tuned for that  $V_{DD}$ , but where frequency is still scalable and thus energy efficiency can still be optimized. We propose a latch-based design method that optimizes the minimum energy-delay curve of a circuit and attempts to perform DVFS energy efficiency with one  $V_{DD}$  by judicial insertion/deletion of pipeline stages based on workload.

## 5.2 Hypothesis

We hypothesize that when considering energy consumed from the DC-DC converter, performing frequency scaling using a single- $V_{DD}$ , latch-based design that judiciously inserts and deletes pipeline stages is more energy efficient than the recently published multi- $V_{DD}$  domain DVFS solution for a certain range of frequency.

## 5.3 Approach

### 5.3.1 Related Work

Since there are three main aspects to this project: DC-DC converter efficiency, DVFS schemes, and latch-based digital design, a literature study was done on each. [43][44] provide overview and a specific implementation of DVFS for reference. [45][46] present reputable DC-DC converter efficiencies suitable for ULV designs, and those respective efficiencies will be incorporated into the evaluation of the design proposed. [47-50] discuss issues and methods for designing with latch-based timing. [51][52] provide a model for optimal pipelining of circuits, which will be an important aspect of our design. Finally, [53] shows how optimal pipelining of latch-based circuit can further decrease the minimum energy point.

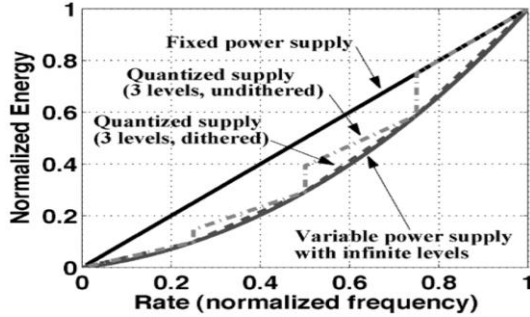


Figure 23. Theoretical energy consumption versus rate for different power supply strategies. Figure taken [43].

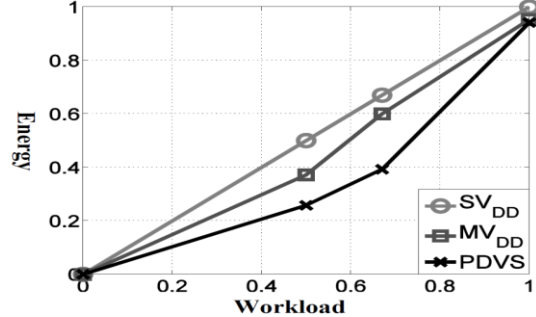


Figure 24. Measured average energy vs. workload published in [44].

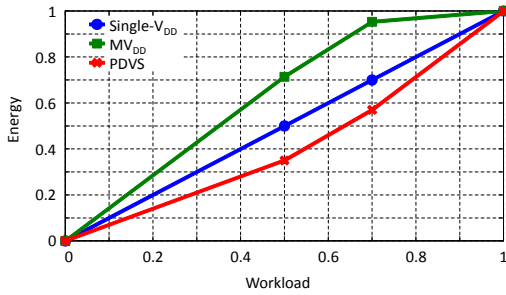


Figure 25. Energy ‘savings’ of multi- $V_{DD}$  and PDVS schemes with considerations of DC-DC converter efficiency  $\eta=0.7$ .

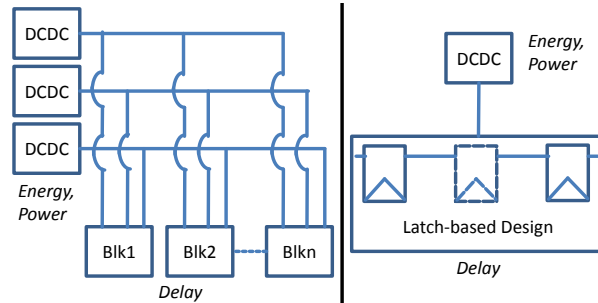


Figure 26. Diagram of our comparison cases between PDVS vs. proposed. Evaluation of energy/power consumption should come from the DC-DC converter.



### 5.3.2 Proposed Research Steps

Fig. 27 shows an overview of the idea presented in this Chapter. We propose a ‘DVFS’ scheme where we use one  $V_{DD}$ , but frequency can still be scaled depending on workload by having logic switches that insert or take away pipeline stages. The question then, is if and how these scheme may save energy similar to PDVS[44] schemes. First, we will perform a case study on how latches help make possible the

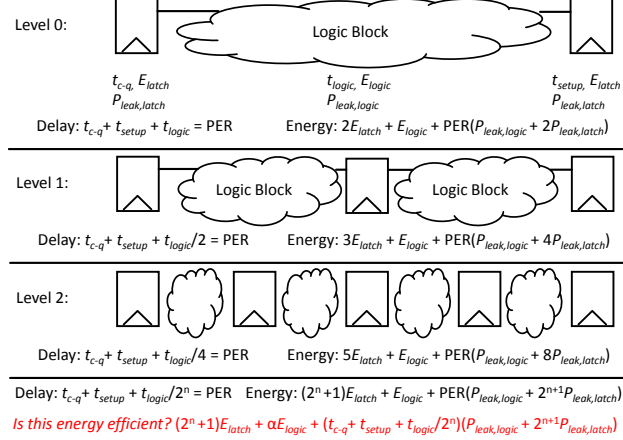


Figure 27. Breakdown and modeling of our proposed latch-based design idea. The final analytical equation is shown on the bottom of the figure in red. Our research question in analytical terms can be expressed as: ‘is each  $E$  found by sweeping  $n$  more efficient to its PDVS counterparts for a given  $f$ ’, where  $\alpha$  is switching factor,  $E$  is the total path energy, and  $n$  is the level of pipelining.

further decreasing of the minimum energy point. Then, we propose to build a model of our design scheme (like shown in Fig. 27), which will provide insight into the various sensitivity knobs our design will face. From this step we will have known what optimization points we need to focus on to make our scheme a success. Third, we will build common digital blocks such as a multiplier, Kogge-Stone adder, FIR, FFT, or circuits from ISCAS benchmarks[54] to evaluate our scheme. We will likely use some conclusions from Chapter 3 on determining what standard cells are needed. Finally, we propose to compare our design scheme with those such as presented in [44], with considerations of the DC-DC converter efficiency (Fig. 26) and a frequency range achievable by both circuit designs.

### 5.4 Goals and Anticipated Results

So far a study of latches vs. registers has been done, and it has been found that latches are truly superior to registers in terms of energy and delay. Fig. 28 shows some results of this study. The left latch TLAT\_SP, has been custom sized for sub- $V_t$  so that delays for ‘0’ and ‘1’ data balance. Fig. 29 shows an example where such latch replacement is used in an 8-b high speed adder. The E-D curve shifts to the lower left, signifying savings in delay and energy in circuits as well. The next planned step for this project

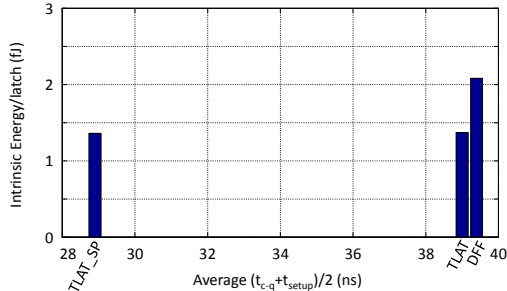


Figure 28. Energy and delay savings of using latches compared to registers. Simulation results for intrinsic energy and delay for same drive strength.

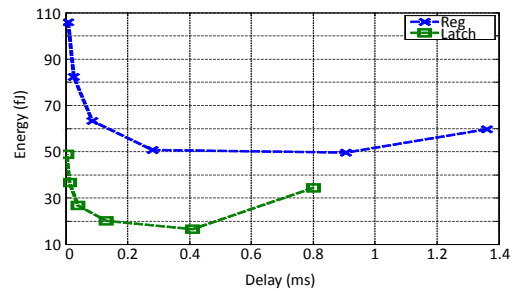


Figure 29. Example shift of E-D curve by using latches replacing registers. E-D curve for 8-b high-speed adder.  $V_{DD}$  swept from 0.25V to 0.5V.

is to implement the model in Fig. 27 by replacing the ‘logic blocks’ with inverter chains with variable switching factor  $\alpha$  (so in reality, the gates will be NAND2 gates with one input either tied to  $V_{DD}$  or

GND). Thus, we will attain simulation results to evaluate the analytical equation in question, which is the next goal for this project. Other goals for this project are to design a circuit implementing the proposed 'DVFS' scheme, and evaluating it against state-of-the-art DVFS solutions with respect to energy efficiency for given frequency constraints in a range achievable by both circuits.

The results of this project should prove useful in many full SoC design deployments, where local components than need DVFS can be implemented in a localized, synthesis flow friendly, and energy efficient manner. In the BASN chip, many blocks such as the FIR or MCU would gain more flexibility in data processing with an increased range of operating frequency for increased energy efficiency.

## 6 Research Tasks

Tasks and timeline of each research goal are listed in Table 2.

**Table 2.** Research Tasks and Timeline, \*=*optional tasks*

PROJECT	#	DESCRIPTION	OUTCOME	TIMELINE
BASN chip Chapter 2	1	Design of architecture of BASN chip	BASN chip architecture	<i>Completed</i>
	2	Tapeout of BASN chip	Tape out chip for measurement	<i>Completed</i>
	3	Chip testing of BASN chip	Measured results for chip	<i>Completed</i>
	4	<b>Paper writing for BASN chip</b>	<b>Publication for BASN chip (in ISSCC)</b>	<i>Completed</i>
	5	Design for NVM memory chip	Architecture improved with 'resurrection' capability	<i>Completed</i>
	6	Tapeout of NVM memory BASN chip	Tape out chip for measurement	<i>Completed</i>
	7	Testing of NVM memory BASN chip	functional NVM for 'resurrection' feature	<i>In progress</i>
	8	<b>Paper writing for NVM memory chip</b>	<b>Publication for NVM 'resurrection' feature</b>	10/2012-11/2012
Library Design and Characterization at ULVs for Robust Timing Closure	1	Design of pass-transistor based NOR2 gate for evaluation	Understand if pass-transistors will work	03/2012-05/2012
	2*	Expand design into sub-Vt library with different drive strength*	Standard cell library building	05/2012-10/2012
	3*	Expand design into sub-Vt library with different lengths*	Standard cell library with cells for leakage optimization	05/2012-12/2012
	4	<b>Writing of cell design methodology for sub-Vt</b>	<b>Publication for pass-transistor cell design</b>	05/2012
	5	Synthesis run to verify sub-Vt library	Verification this library will work for real designs	12/2012
	6	<b>Writing of synthesis gate replacement for leakage optimization</b>	<b>Publication for leakage saving design flow idea</b>	12/2012
	7	Script to do gate replacement with our library	First major step of whole flow complete	01/2013
	8*	Clock network extraction and retiming*	Full synthesis flow done	1/2013-2/2013
	9*	Circuit benchmark verification, tapeout such blocks*	Tapeout	2/2013-3/2013
	10*	Chip testing*	Measured results	08/2013
	11*	<b>Writing of whole flow*</b>	<b>Publication for block synthesis design method for sub-Vt</b>	09/2013

Hold Time Analysis and Timing Closure  Method for Sub-Threshold	1*	Design robust and suitable register for hold time*	Robust hold time register	03/2012
	2	Analysis of variables	Wholesome design methodology for hold time	04/2012-05/2012
	3*	Modeling of novel two-phase method*	Model for feasibility of novel idea	05/2012-09/2012
	4	Exploration of design space for suitable DLL	Suitable DLL to be used in design space	09/2012
	5*	Design DLL*	DLL done	09/2012-11/2012
	6	<b>Writing of analysis of variables</b>	<b>Publication on optimal hold time design method for sub-Vt</b>	10/2012
	7	Come up with methodology on using novel two-phase idea	Methodology done	11/2012-12/2012
	8	Evaluate this design compared to conventional methods	Comparison done	01/2013
	9*	<b>Writing of DLL design for sub-Vt*</b>	<b>Publication on low power DLL</b>	01/2013
	10*	Tapeout this design*	Tapeout	02/2013
	11*	Chip testing*	Measured results	08/2013
	12*	<b>Writing of novel two-phase method*</b>	<b>Publication for novel two-phase clock method</b>	10/2013
Latch Based Design for Single-VDD Alternative Approach to DVFS	1	Latch based synthesis flow exploration	Latch based synthesis flow	<i>Completed</i>
	2	Model evaluation	Evaluation of model, identified key sensitivity factors	03/2012-05/2012
	3	Design methodology for optimal pipelining using adders	Latch based minimum energy point methodology	09/2012-12/2012
	4	Expansion of method for DVFS capabilities	Evaluate if this 'DVFS' alternative will work	01/2013
	5	<b>Writing of latch based minimum energy point analysis</b>	<b>Publication on latch based design method</b>	01/2013
	6	Expand designs to larger blocks, like multipliers or FFTs	Bigger block designs	01/2013-3/2013
	7*	Tapeout those designs*	Tapeout	03/2013
	8	<b>Writing of DVFS alternative method</b>	<b>Publication on proposed method based on sim results</b>	05/2013
	9*	Chip testing*	Measured Results	08/2013
	10*	<b>Writing of method with chip results*</b>	<b>Publication on proposed method based on measurements</b>	09/2013
Thesis Writing	1	Finish any chip measurements and publications needed	Finish all chip measurements and publications	10/2013
	2	Write thesis, await publication accepts/rejects	Thesis written	11/2013
	3	PhD defense	Graduate	12/2013

## 7 List of Current Publications

1. Fan Zhang, **Yanqing Zhang** et al., "A Batteryless 19 $\mu$ W MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC", to appear in *2012 International Solid-State Circuits Conference*, 02/2012.

2. Benton H. Calhoun et al., “Body Sensor Networks: A Holistic Approach from Silicon to Users”, *IEEE Proceedings*
3. **Yanqing Zhang** and Benton H. Calhoun, “The Cost of Fixing Hold Time Violations in Sub-threshold Circuits”, *2011 Subthreshold Microelectronics Conference*, 09/2011
4. **Yanqing Zhang** et. al., “Energy Efficient Design for Body Sensor Nodes”, *Journal of Low Power Electronics and Applications*, 04/2011.
5. Benton H. Calhoun, Sudhanshu Khanna, **Yanqing Zhang**, Joseph Ryan, and Brian Otis, “System Design Principles Combining Sub-threshold Circuits and Architectures with Energy Scavenging Mechanisms”, *International Symposium on Circuits and Systems (ISCAS)*, Paris, France, pp. 269-272, 05/2010.

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- [3] D. Yeager, F. Zhang, A. Zarrasvand, and B. P. Otis, "A 9.2 $\mu$ A Gen 2 Compatible UHF RFID Sensing Tag with -12dBm Sensitivity and 1.25 $\mu$ Vrms Input-Referred Noise Floor", *2010 International Solid-State Circuits Conference*, Feb 2010.
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